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High Speed Direct Signal Frequency Synthesizer

D. Haribabu
Associate Prof., Noble College of Engineering and Technology for Women Nadergul, Hyderabad
babuhari81@gmail.com

D. Brahmanandam
Mallareddy Institute of Technology, Maisammaguda,Hyderabad

***Abstract* – Frequency synthesizers are very critical blocks for embedded systems in communications and instrumentation applications. Direct Digital Frequency synthesis is widely used technique, due to its high frequency resolution and fast switching between frequencies over a large bandwidth of interest. The DDFS in modulator mode can be used for producing ASK, FSK and PSK signals. In pattern generation mode the DDFS can be used to generate sine, square, triangular and arbitrary waveforms.**

***Keywords* – Frequency synthesizers, DDFS.**

I. INTRODUCTION

1.1 Frequency Synthesis various methods

The term "**frequency synthesis**" applies to a technique that accepts some reference input and then generates one or more signals of predefined type as according to a control word or method. The stability, accuracy, and spectral purity are the performance measures of frequency synthesizer.

1.2 DDFS basic principle

Direct Digital Frequency Synthesizer is a technique to produce desired output waveforms with full digital control (hence also called Numerically Controlled Oscillator). Direct digital synthesis (DDS) is becoming increasingly popular as a technique for frequency synthesis, especially if high frequency resolution and fast switching between frequencies over a large bandwidth are required.

In DDFS, the instantaneous phase of a sinusoidal signal is given by a number stored in a digital accumulator. The accumulator is incremented by adding a constant amount at each clock period, its content will represent a phase value which increases linearly with time. When the accumulator exceeds a value equivalent to 2π radians, it overflows, multiples of 2π are discarded, and the incrimination process continues to the next cycle. The number held in the accumulator is used to address a look-up table held in ROM (read- only memory) which converts phase information to a series of discrete, digitized samples of the amplitude of a sine-wave. A DAC (digital-to-analogue converter), followed by a low-pass filter, convert the digital samples into an analogue signal. Different Look Up Tables (LUT) can be used to produce desired output waveform such as square wave and triangular wave etc.The direct digital frequency synthesizer is shown in a simplified form in Figure 1.2. The DDFS has the following basic blocks;

(1) Frequency register
(2) Adder and phase register
(3) Phase to amplitude converter (conventionally a sine ROM)
(4) Digital to Analog converter and Low pass filter

The phase accumulator consists of a *j*-bit frequency register, which stores a digital phase increment word followed by a *j*-bit full adder and a phase register. The digital input phase increment word is entered in the frequency register. At each clock pulse this data is added to the data previously held in the phase register. The phase increment word represents a phase angle step that is added to the previous value at each 1/*fclk* seconds to produce a linearly increasing digital value. The phase value is generated using the modulo 2^j overflowing property of a *j*-bit phase accumulator. The rate of the overflows is the output frequency.

$$f_{out} = \frac{\Delta P f_{clk}}{2^j} \qquad \forall \quad f_{out} \le \frac{f_{clk}}{2},$$

Where Δ*P* is the phase increment word, *j* is the number of phase accumulator bits, f_{clk} is the clock frequency and f_{out} is the output frequency. The constraint for maximum value of f_{out} in the above equation comes from the sampling theorem.

The phase increment word in (1.1) is an integer, therefore the frequency resolution is found by setting Δ*P* = 1.

$$\Delta f = \frac{f_{clk}}{2^j}.$$

This corresponds to the smallest frequency change that the DDFS can produce. This also corresponds to the lowest frequency that can be produced by the DDFS for a given value of f_{clk} and j (number of bits).

The read only memory (ROM) is a sine look-up table, which converts the digital phase information into the values of a sine wave. In the ideal case with no phase and amplitude quantization, the output sequence of the table is given by

$$\sin(2\pi \frac{P(n)}{2^j}),$$

where *P*(*n*) is a (the *j*-bit) phase register value (at the *n*th clock period). The numerical period of the phase accumulator output sequence is defined as the minimum value of *Pe* for which *P*(*n*) = *P*(*n*+*Pe*) for all *n*. The numerical period of the phase accumulator output sequence (in clock cycles) is

$$Pe = \frac{2^j}{\mathrm{GCD}(\Delta P, 2^j)},$$

where GCD (Δ*P*, 2^j) represents the greatest common divisor of Δ*P* and 2^j. The numerical period of the sequence samples recalled from the sine ROM will have the same value as the numerical period of the sequence generated by the phase accumulator. Therefore, the spectrum of the output waveform of the DDS prior to a digital-to-analog

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conversion is characterized by a discrete spectrum consisting of *Pe* points. The ROM output is presented to the D/Converter, which develops a quantities analog sine wave. The D/A-converter output spectrum contains frequencies *nfclk ± fout*, where *n* = 0, 1 …etc. The amplitudes of these components are weighted by a function.

$$\sin c(\frac{f}{f_{clk}}).$$

This effect can be corrected by an inverse sinc(*f*/*fclk*) filter. The filter that is after the D/A converter removes the high frequency sampling components and provides a pure sine wave output.

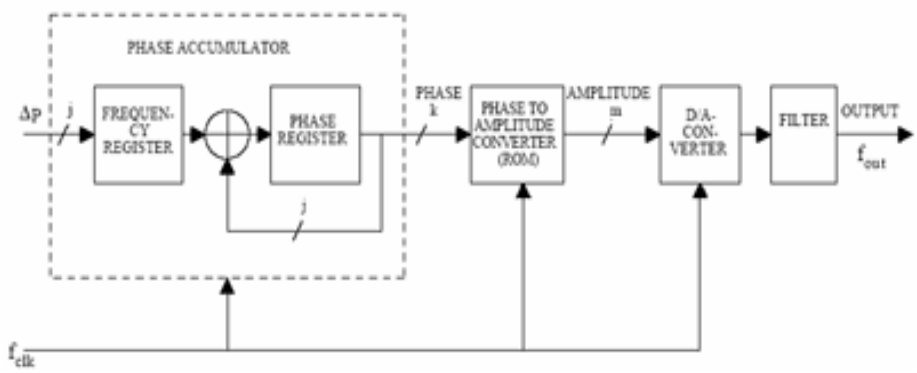

Fig.1. Basic Block Diagram of DDFS

As the DDS generates frequencies close to *fclk*/2, the first image (*fclk* - *fout*) becomes more difficult to filter. This results in a narrower transition band for the filter. The complexity of the filter is determined by the width of the transition band. Therefore, in order to keep the filter simple, the DDS operation is limited to less than 40 percent of the clock frequency.

2. DDFS Architecture for Modulation Capability

It is simple to add modulation capabilities to the DDS, because the DDS is a digital signal processing device. In the DDS it is possible to modulate numerically all three waveform parameters

$$s(n) = A(n) \sin (2 \pi (\Delta P(n) + P(n)))$$

Where *A*(*n*) is the amplitude modulation, Δ*P*(*n*) is the frequency modulation, and *P*(*n*) is the phase modulation. All known modulation techniques use one, two or all three basic modulation types simultaneously. Consequently any known waveform can be synthesized from these three basic types within the Nyquist band limitations in the DDS. Figure 2.1 shows a block diagram of a basic DDS system with all three basic modulations in place .

The frequency modulation is made possible by placing an adder before the phase accumulator. The phase modulation requires an adder between the phase accumulator and the phase to amplitude converter. The amplitude modulation is implemented by inserting a multiplier between the phase to amplitude converter and the D/A-converter. The multiplier adjusts the digital amplitude word applied to the D/A-converter. Also, with some D/A-converters it is possible to provide an accurate analog amplitude control by varying a control voltage.

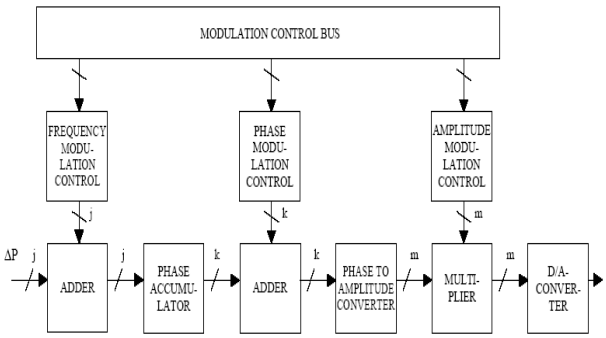

Fig.2.1 DDS Architecture with Modulation Capabilities

II. Implementation of Basic Blocks of DDFS

The basic block diagram of DDFS implemented is shown in the below Fig.3.1. All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an Analog Digital converter must be used to digitize the modulating signal which can be used in DDFS.

III. DDFS Applications

Direct Digital Frequency Synthesis (DDFS) makes it possible to generate single phase or quadrature sinusoids over bandwidths measured in hundreds of megahertz, with sub-hertz frequency resolution, unparalleled frequency hopping rates, and phase continuity on hopping. These characteristics make DDF Synthesizers ideal in a wide

array of applications, including spread-spectrum communications, radar, instrumentation and broadcasting. Design challenges include maintaining high spectral purity, high clock rates and low power consumption.

(1) DDFS is higly preferred option in Instrumentation for signal generation and frequency sweep etc. In the present technology several types of signal generators, Oscilloscopes, function generators and spectrum Analyzers use high quality DDFS circuits to achieve accurate and precise frequency/phase control.
(2) DDFS can be efficiently used in several Digital modulation schemes such as Frequency Shift Keying, Phase Shift Keying and Amplitude Shift Keying.
(3) The digital structural nature of DDFS allows designers to add programmability in it which makes DDFS suitable for custom communication and Instrumentation applications.
(4) DDFS is capable of well controlled, rapid changes in frequency, over a relatively large frequency range, makes it attractive for mobile communication systems such as Blue tooth etc.
(5) DDFS has been used in Universal HAM radio/generator DDS Unit(along with AD9850 or AD9851)
(6) Timing signal generator employing direct digital frequency synthesis.

A timing signal generator including a direct digital frequency synthesizer (DDFS), a divide-by-N counter, and a pattern generator, produces a TIMING signal conveying a timed sequence of pulses. The pattern generator produces a sequence of data pairs (FREQ,N), with each pair being produced in response to each pulse of the TIMING signal and indicating a time interval that is to occur between that TIMING signal pulse and a next TIMING signal pulse. The DDFS produces an output sine wave signal (SINE) having a frequency controlled by the current FREQ data output of the pattern generator. The divide-by-N counter produces the timing signal pulses. It counts cycles of the SINE signal occurring since it last produce a TIMING signal pulse and generates a next TIMING signal when it has counted the number of SINE signal pulses indicated by the current N data output of the pattern generator.

3.1 Instrumentation Applications

An important and growing DDS market segment: is instrumentation. Various instruments have exploited a DDS during the past decade, with varying degrees of success. In some, the DDS is the sole signal generation circuit. In others the DDS is used to augment or simplify either a PLL or a mix/filter/divide circuit. Two new generations of DDS instrumentation are now emerging. One uses a DDS as the basic signal generator, usually built as one or more ASICs, plus intelligence.

The most aggressive instrumentation application contemplated for new DDS designs will be an instrument based on the new wideband DDS In fact, there are no other approaches that permit broadband synthesized "chirp" and sweep functions, or Doppler simulation. Overall, the market for DDS-based instruments is viewed as good and growing.

IV. LIMITATIONS OF DDFS

(1) Spurious products is a prime limitation of DDS. There are mainly four sources of spurious products in a DDS:

- The value of instantaneous phase given by accumulator is truncated to match the address word-length of the ROM.
- Amplitude quantization in the ROM.
- Data compression implemented in the ROM to maximize the output frequency by minimizing the size of the ROM.
- Imperfections in the DAC such as non-linearity's, glitches due differences in on/off switching, switching time disparities between bits, and limited settling-time

(2) Another important limitation, due to Nyquist's sampling theorem, requires the maximum output frequency to be less than half the clock frequency. Synthesizer design is thus a trade-off between having a large, spurious-free, dynamic range and having a high speed, the former requiring reduced phase truncation, gained at the expense of a large, slow, ROM. The digital parts of the circuit are generally designed with a resolution small enough that the spurious-free dynamic range is determined by the properties of the DAC.

V. RESULT

5.1 Spectral Analysis

DDFS is tested with delta phase value "00000100". The outputs obtained from DDFS are plotted in time domains are shown in figure 5.1. The FFT of amplitude values are computed using a MATLAB program. The output FFT graph is shown in figure 5.2. It can be observed that the output peaks at the fundamental frequency showing negligible harmonic distortion.

It can be observed that the FFT peaks at index 16, this is corresponding to the output signal frequency which is clock frequency divided by 16.

DDFS can be operated in the following three modes

a) Basic Mode: I and Q carrier signals for a chosen freq value

b) Modulator Mode: producing ASK, FSK and PSK signals.

c) Pattern Generation Mode: generates sine, square, triangular and arbitrary waveforms

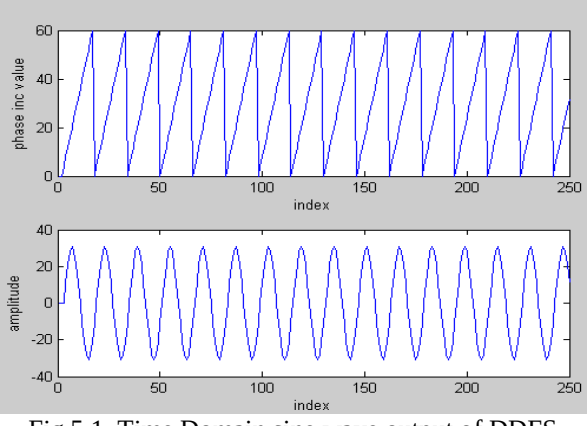

Fig.5.1. Time Domain sine wave output of DDFS

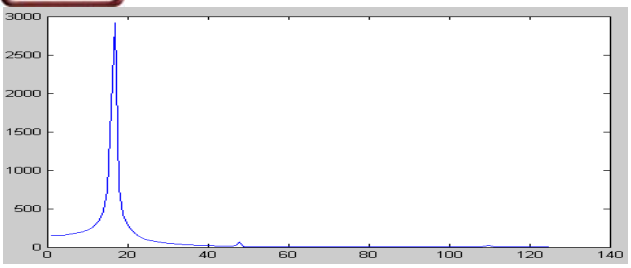

Fig.5.2. FFT on the DDFS output for frequency of sampling F_s divided by 16

1 DDFS Simulation for various output frequencies (ASK,PSK, FSK)

DDFS can produce different output frequencies based on the delta phase value input (assuming no frequency modulation). The minimum delta phase value that can be loaded into DDFS is "00000001", which causes the phase increment of one for each clock pulse. Hence the resulting signal has 256 samples in each cycle. This also implies that the output frequency is 1/256 times of clock frequency.

The maximum value delta phase value that can be loaded in DDFS is "10000000", which results in output signal with two samples for each cycle. This also implies that the resulting signal frequency is ½ times of clock signal frequency (In practical conditions more that 0.4 times of clock signal frequency can't be achieved due to several reasons. These issues are not considered in this project). Below figure shows Modulator Mode Outputs Producing ASK, FSK and PSK signals.

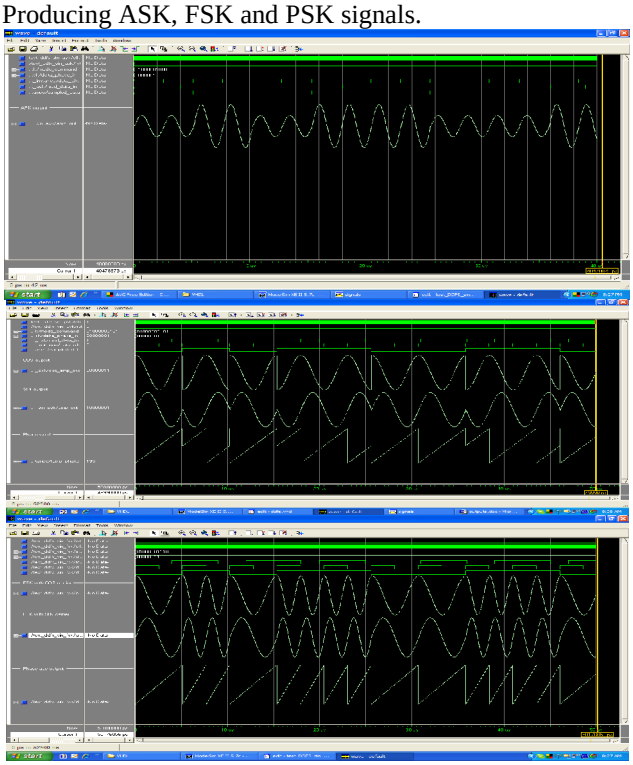

Fig.5.3 DDFS PSK,FSK signals

Highest clock frequency observed from timing analyzer is 50 MHz

Hence the maximum frequency that can be obtained is half of this value.

DDFS maximum output signal frequency is 25 MHz

Minimum frequency is = 50MHz/256 MHz

= 0.1953125MHz

Operating Frequency	Expected Frequency	Simulated Frequency	Difference	% of Error
500MHz	7.324219	7.324400	182	0.002%
750MHz	10.98623	10.981800	4528	0.041%
1GHz	14.648438	14.630500	17937	0.123%

Table 5.1 : Basic DDS Frequency Table

VI. CONCLUSIONS

A Major advantage of a direct digital synthesizer (DDS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital control. Other inherent DDS attributes include the ability to tune with extremely fine frequency and phase resolution. In current technology DDFS is a viable alternative to analog based phase-locked loop (PLL) technology for generating agile analog output frequency in consumer synthesizer applications.

It is easy to include different modulation capabilities in the DDS by using digital signal processing methods, because the signal is in digital form. By programming the DDS. The flexibility of the DDS makes it ideal for different types of signal generators. The digital circuits used to implement signal-processing functions do not suffer the effects of thermal drift, aging and component variations associated with their analog counterparts. The implementation of digital functional blocks makes it possible to achieve a high degree of system integration. Recent advances in IC fabrication technology, particularly CMOS, coupled with advanced DSP algorithms and architectures are providing possible single-chip DDFS solutions to complex communication and signal processing subsystems as modulators, demodulators, local oscillators (LOs), programmable clock generators, and chirp generators. The DDS addresses a variety of applications, including cable modems, measurement equipments, arbitrary waveform generators, cellular base stations and wireless local loop base stations.

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AUTHOR'S PROFILE

Mr. D. Hari Babu
obtained his B. Tech. from Narayana Eng. College, Nellore., M.Tech from JNTUH, Hyderabad. He is having 9 years of experience. His research areas and publications include signal processing, Adaptive Signal Processing, Advance communications. Presently Working as Associate Professor in Noble College of Engineering and Technology for Women, Nadergul.

Mr. D. Brahmanandam
Working as Assistant Professor in Mallareddy Institute of technology, Hyderabad. He is having 3 years of experience. His research areas and publications include signal processing , Electromagnetic waves.